

In the Claims

The claims are as follows:

1 1.-20. (Cancel)

2 21. (Original) An isolation structure in a semiconductor substrate comprising:

3 a semiconductor substrate;

4 a plurality of adjacent trenches in said semiconductor substrate; and

5 a self-aligned isolation structure in upper portions of selected ones of said

6 plurality of trenches, said isolation structure being merged portions of

7 said semiconductor substrate along at least a first row of said selected

8 ones of said plurality of adjacent trenches, said merged portions of said

9 semiconductor substrate being aligned as-formed to edges of said

10 plurality of adjacent trenches,

11 wherein said self-aligned isolation structure isolates a first region of said

12 semiconductor substrate from a second region of said semiconductor substrate.

1 22. (Currently amended) The structure ~~apparatus~~ of claim 21 wherein said

2 semiconductor substrate comprises a silicon substrate.

1 23. (Currently amended) The structure ~~apparatus~~ of claim 21 further including

2 a pad dielectric layer thereover a surface of said semiconductor substrate.

1 24. (Currently amended) The structure ~~apparatus~~ of claim 23 wherein said pad
2 dielectric layer comprises a pad oxide layer followed by a pad nitride layer.

1 25. (Currently amended) The structure ~~apparatus~~ of claim 24 wherein said pad
2 oxide layer has a thickness ranging from about 1 nm to about 10 nm.

1 26. (Currently amended) The structure ~~apparatus~~ of claim 24 wherein said pad
2 nitride layer has a thickness ranging from about 50 nm to about 500 nm.

1 27. (Currently amended) The structure ~~apparatus~~ of claim 21 wherein said
2 plurality of adjacent trenches have depths ranging from about 250 nm to about
3 10 μ m.

1 28. (Currently amended) The structure ~~apparatus~~ of claim 21 wherein said self-
2 aligned isolation structure comprises a thermal oxide region existing along said at
3 least first row of selected ones of said plurality of adjacent trenches.

1 29. (Currently amended) The structure ~~apparatus~~ of claim 28 wherein said
2 semiconductor substrate comprises a silicon substrate and said thermal oxide
3 region comprises a thermal silicon dioxide region existing along said at least first
4 row of selected ones of said plurality of adjacent trenches.

- 1 30. (Original) An isolation structure in a semiconductor substrate comprising:
2 a silicon substrate having a layer of pad oxide disposed thereover said silicon
3 substrate and a layer of pad nitride disposed thereover said pad oxide;
4 a plurality of adjacent trenches traversing through said pad oxide, said pad
5 nitride, and stopping in said silicon substrate; and
6 a self-aligned, thermal oxide isolation structure in upper portions of said
7 plurality of adjacent trenches, said thermal oxide isolation structure being
8 oxidized portions of said semiconductor substrate merged along at least a
9 first row of selected ones of said plurality of adjacent trenches in said
10 upper portions of said trenches, said oxidized portions of said
11 semiconductor substrate being aligned as-formed to edges of said
12 plurality of adjacent trenches,
13 wherein said thermal oxide isolation structure isolates a first region of said
14 semiconductor substrate from a second region of said semiconductor substrate.

Please add new claims 31-40 as follows:

- 1 31. (New) An isolation structure in a semiconductor substrate comprising:
2 a semiconductor substrate;
3 a plurality of adjacent trenches in said semiconductor substrate

4 a plurality of adjacent segments of said semiconductor substrate between each
5 of said plurality of adjacent trenches;
6 an oxidation barrier layer residing in lower portions of said plurality of adjacent
7 trenches;
8 a self-aligned shallow trench isolation comprising merged sections of selected
9 ones of said plurality of adjacent segments of said semiconductor substrate
10 along a first row above said oxidation barrier layer.

1 32. (New) The structure of claim 31 wherein said semiconductor substrate
2 comprises a silicon substrate.

1 33. (New) The structure of claim 31 further including a pad dielectric layer
2 thereover a surface of said semiconductor substrate.

1 34. (New) The structure of claim 33 wherein said pad dielectric layer
2 comprises a pad oxide layer followed by a pad nitride layer.

1 35. (New) The structure of claim 31 wherein said oxidation barrier layer is a
2 material selected from the group consisting of local oxidation of silicon, silicon
3 nitride and silicon oxynitride.

1 36. (New) The structure of claim 33 wherein said oxidation barrier layer has a
2 thickness ranging from about 2nm to about 50nm.

1 37. (New) The structure of claim 31 wherein said plurality of adjacent trenches
2 have depths ranging from about 250 nm to about 10 μ m.

1 38. (New) The structure of claim 31 wherein said self-aligned isolation
2 structure comprises a thermal oxide region existing along said at least first row of
3 selected ones of said plurality of adjacent trenches.

1 39. (New) The structure of claim 38 wherein said semiconductor substrate
2 comprises a silicon substrate and said thermal oxide region comprises a thermal
3 silicon dioxide region existing along said at least first row of selected ones of said
4 plurality of adjacent trenches.

1 40. (New) The structure of claim 31 wherein said selected ones of said
2 plurality of adjacent segments of said semiconductor substrate comprise those
3 adjacent segments of said semiconductor substrate along said at least first row
4 having a thinned diameter ranging from about 1/5 to about 1/2 that of a non-
5 thinned, original diameter of said plurality of adjacent segments of said
6 semiconductor substrate.